which is then reduced to between about 2000 to 6000 Å after chemical-mechanical polishing. Thus, when, at the next step, nitride layer (220) is removed, a deep opening (235) is left behind. Nitride removal is accomplished using phosphoric acid, H_3PO_4. Pad oxide layer (210) underlying nitride layer (220) is also removed preferably by using wet etch, thus leaving openings (235) in between the isolation oxide "caps" (250) that protrude above the STI (230).

IN THE CLAIMS

Claims 1 and 5 have been amended as follows:

29. (AMENDED ONCE) A stacked-gate flash memory having a shallow trench isolation with a high-step oxide and high lateral coupling comprising:

a substrate having a gate oxide layer;

at least two trenches formed to a depth between about 2500 to 5000 Å below the surface of said substrate;

an oxide liner formed over said substrate, including over the inside walls of said two trenches;

a high-step oxide formed within said two trenches over said oxide liner and protruding upward over the surface of said substrate to a height between about 2000 to 6000 Å;

said high-step oxide forming an opening with high walls over the surface of said substrate between said two trenches;

a first polysilicon layer formed conformally inside said opening and over the surface of the substrate between said high walls to form a floating gate having folding surfaces;

an intergate oxide formed over said floating gate having folding surfaces;

a second polysilicon layer formed protruding downward in between said folding surfaces over said intergate oxide layer to form a control gate; and

a self-aligned source (SAS) line.

Claim 30, please cancel.

Claim 31, please cancel.

Claim 32, please cancel.

33. (AMENDED ONCE) The stacked-gate flash memory cell of 29, wherein said opening has a width between about 1500 to 5000 Å.

34. (AMENDED ONCE) The stacked-gate flash memory cell of 29, wherein said first conductive layer is polysilicon having a thickness between about 100 to 500 Å.

35. (AMENDED ONCE) The stacked-gate flash memory cell of 29, wherein said second conductive layer is polysilicon having a thickness between about 1000 to 3000 Å.